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The Clock and Control System for the EuXFEL 2D Detectors: Firmware and System Integration

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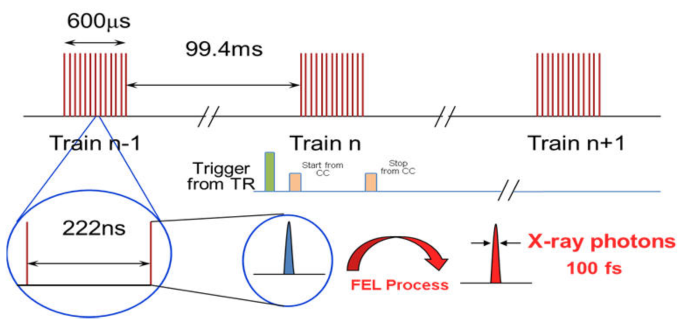
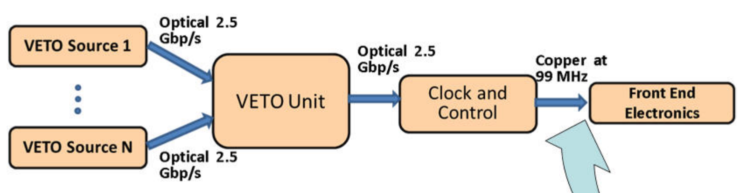
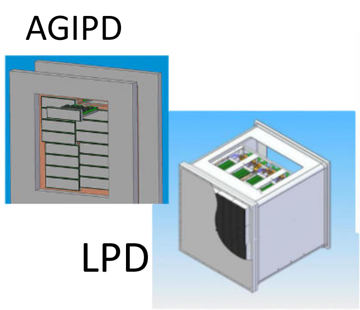
UCL

For the European Free Electron Laser (EuXFEL), in normal operation, 27 000 electron bunches are generated per second, grouped into 10 trains of 2 700 bunches with an inter bunch time separation of 220 ns which corresponds to a frequency of 4.5 MHz. The lasing generated from 20 mm electron bunches provides short X-ray flashes of <100 fs duration. This requires that all control and data taking electronics have to cope with 4.5 MHz bunch delivery rates interspersed by 99.4 ms inactivity periods.



Each generated X-ray flash is intense enough to produce a full diffractive picture of scattering targets. Three different 2D detector designs are in development, namely, AGIPD, DSSC and LPD. The clock and control (CC) system is a part of the rack mounted electronics for the DAQ system which constitutes the interface between the overall EuXFEL timing and the Front End Electronics (FEEs).





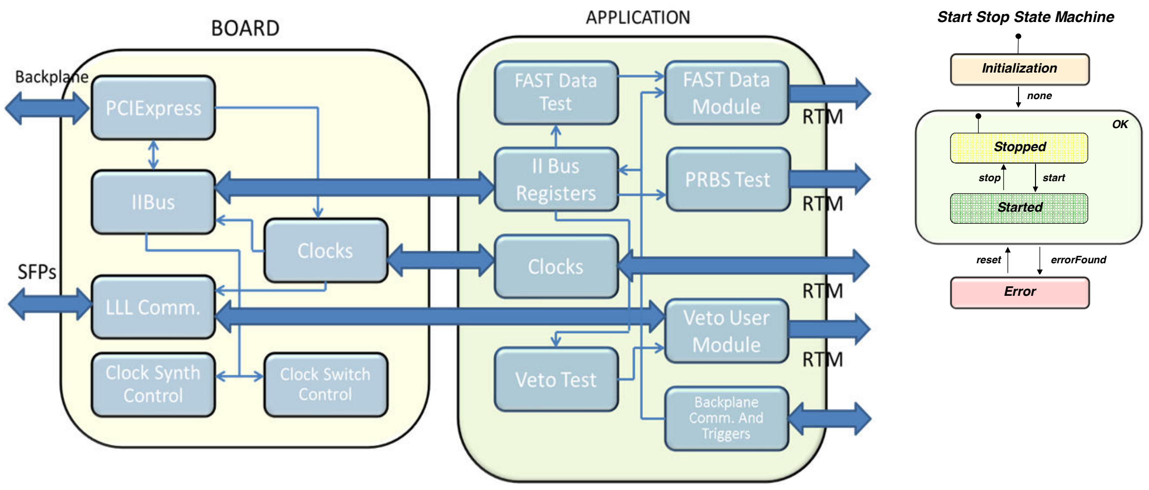
VETO MESSAGES TO THE FEE UNITS

Command	Start Bits	Payload	Purpose
VETO	110	Bunch ID (12 bits) + 0000	Identifies bunch ID to be vetoed
NO VETO	101	Bunch ID (12 bits) + 0000	No veto defined for that bunch ID
GOLDEN	111	Bunch ID (12 bits) + 0000	Identifies bunch as golden
Reserved	100	Bunch ID (12 bits) + 0000	

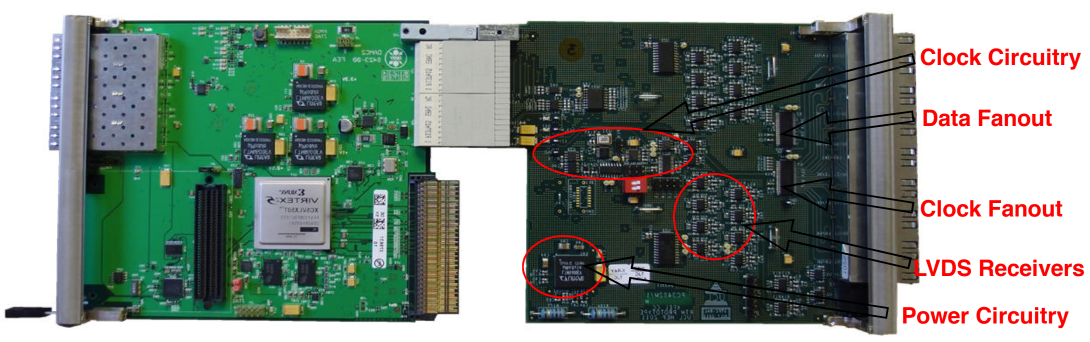
FAST MESSAGES TO THE FEE UNITS

Command	Start Bits	Payload	Purpose
START	1100	Train ID (32 bits) + Shot ID (8 bits) + Checksum (8 bits)	Notifies FEE of coming train
STOP	1010	None	Notifies FEE that the train ended
RESET	1001	None	Reset FEE
Reserved	1111		

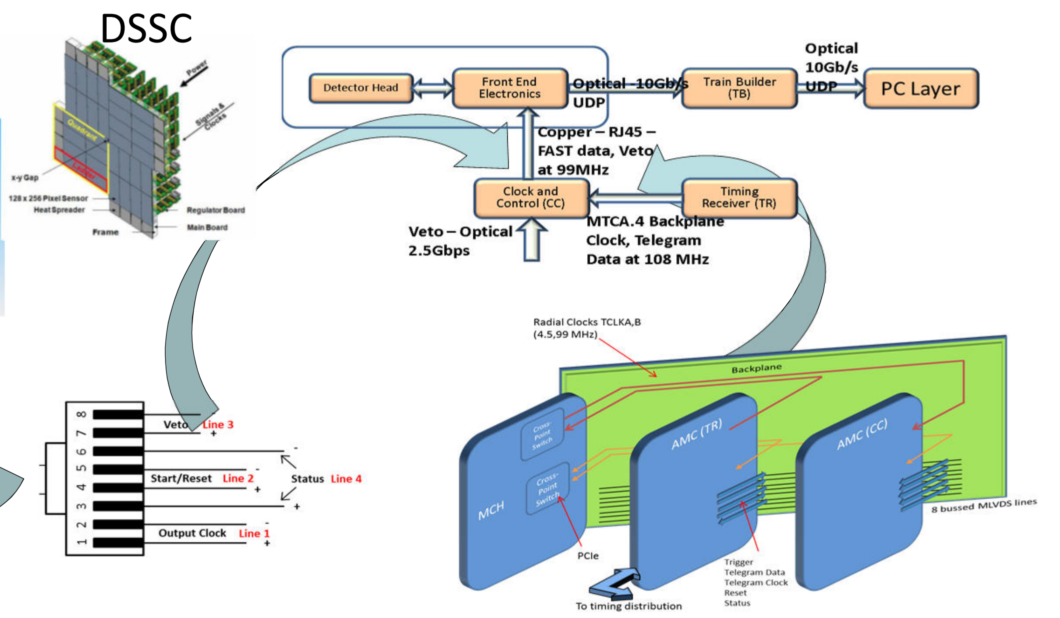
The firmware for the CC system is made up of customised re-usable modules centred around a bus/register structure called IIBus and it appears in the application part of the overall DAMC2 firmware. The main components include the modules for communication with the TR board, the Veto Unit (VU) board, the FEEs, and the crate CPU board. These modules are designed as general purpose drop-in parts that can be customised through the use of generics.



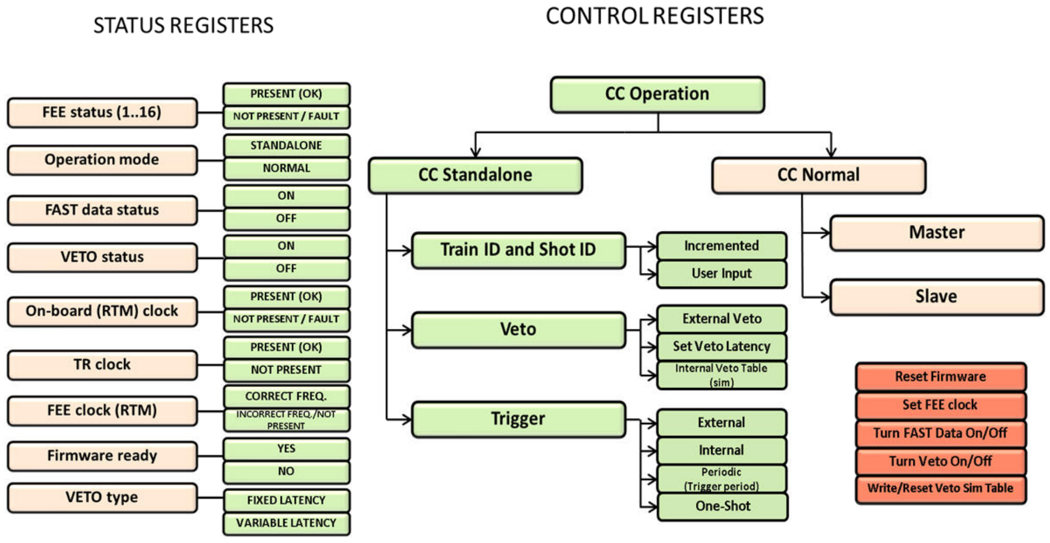
The hardware for the CC system for EuXFEL megapixel detectors is based on a combination of a general purpose MTCA.4 AMC board and a compatible Rear Transition Module. The AMC board is the DESY designed DAMC2, which has a Xilinx V5LX50T FPGA to provide processing power. The RTM is a custom designed PCB that provides the connectivity to the Front End Electronics (FEE) units at the detector end as well as the clock circuitry for the CC system operation.



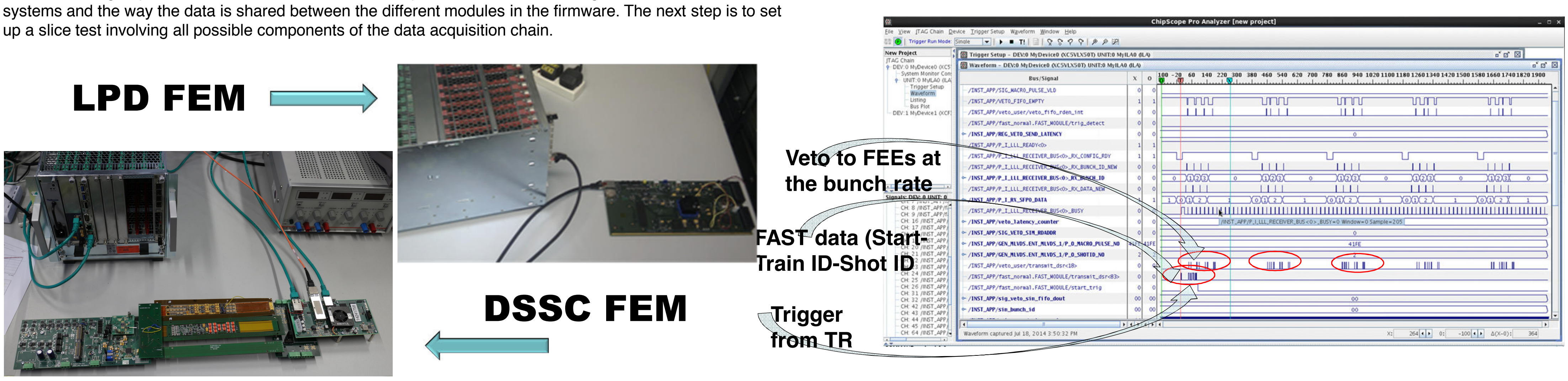
The CC system sits in the same MTCA.4 crate as the timing receiver (TR) board and receives the trigger, the clock and the train ID and the shot ID information (telegram data) over the backplane.



The CC system integrates to the overall EuXFEL DAQ system through the EuXFEL software framework, Karabo. Karabo sees the CC system as a device which is a controllable object with a state machine based program flow having its own graphical user interface. The control of the device is done through accessing the CC registers. The register structure consists of the control and the status parts. The control registers can modify every aspects of the hardware for normal and the test operations.



The integration of the CC system to the EuXFEL software framework has been accomplished seamlessly and the tests are being carried out for integration to the other parts of the EuXFEL system both at UCL and the other detector groups. The results so far show a correct operation in communicating with the various sub-systems and the way the data is shared between the different modules in the firmware. The next step is to set up a slice test involving all possible components of the data acquisition chain.



European XFEL

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