Experiences with the MTCA.4 Solution for the EuXFEL Clock and Control System

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Abstract– The clock and control (CC) system for the EuXFEL megapixel detectors consists of a multi-purpose MTCA.4 AMC card with a Xilinx FPGA and a custom designed Rear Transition Module (RTM) which provides the CC functionality. The system resides in a MTCA.4 crate with the Timing Receiver (TR) board and synchronises the DAQ system to the general EuXFEL timing. This paper presents the experiences with the prototype system in addition to describing the RTM hardware and the CC system firmware in detail. The tests that have been performed to validate the basic MTCA.4 specifications related functionality are presented first. The next stage of tests involve confirming the system functionality by using the TR board as it would be in the EuXFEL DAQ system and a development board to simulate a Front End Electronics (FEE) unit. The performance metrics in terms of jitter and bit error rates for FEE communication are presented. As a result of the performance tests, the improvements and modifications to the current hardware for the final system are outlined in the conclusions.

I. INTRODUCTION

The design and the development of the hardware for the Clock and Control (CC) system for the European Free Electron Laser (EuXFEL) megapixel detectors is described in [1]. The system is based on a combination of a general purpose MTCA.4 AMC board and a compatible Rear Transition Module. The AMC board is the DESY designed DAMC2 [2], which has a Xilinx V5LX50T FPGA to provide processing power and connectivity for different subsystems in the EuXFEL. The RTM is a custom designed PCB that is connected to the AMC via the 60-pin ADF connector which provides up to 54 differential links in addition to the power and the control signals for the MTCA.4 operation. The RTM in turn provides the connectivity to the Front End Electronics (FEE) units at the detector end through the use of a stacked RJ45 connector. Fig. 1 shows the DAMC2 and the CC RTM paired together.

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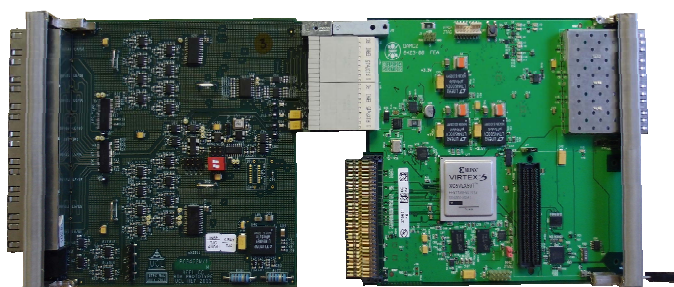
Fig. 1. The CC RTM (left) and the DAMC2 (right) paired together.

The structure of the EuXFEL 2D detector system can be seen in Fig. 2, where the CC system sits in a MTCA.4 crate along with the timing receiver (TR) board and the crate CPU. The timing receiver board is responsible for the synchronisation of the detectors and the DAQ system to the general EuXFEL timing.
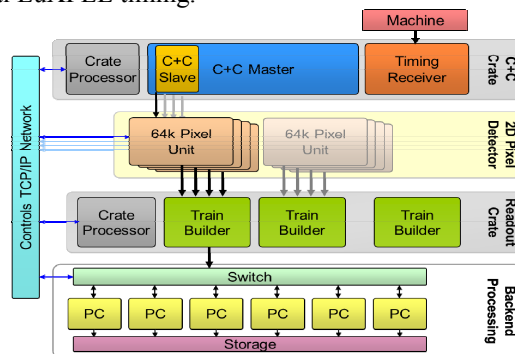

Fig. 2. The structure of the EuXFEL 2D detector readout system.

The EuXFEL facility will generate coherent and intense X-ray flashes with a ~4.5 MHz bunch frequency [3]. The Timing Receiver (TR) board [4], housed in the same crate as the CC system delivers the bunch clock which is the same frequency as the bunch frequency or double that frequency at ~9 MHz to the CC through the MTCA.4 backplane on TCLK1 line [9]. Fig. 3 shows the backplane connections between the TR and the CC system. In addition to the bunch clock, there are backplane MLVDS links to the TR. These links include the Start/Trigger signal which denotes the start of the bunch train, the telegram data that carries the information comprising the current bunch train ID and the bunch pattern index, and the 130 MHz telegram clock to which the telegram data is sent synchronously. Additionally, extra connections also exist on the bussed MLVDS links for various functions such as resetting the CC system and status from the CC system.
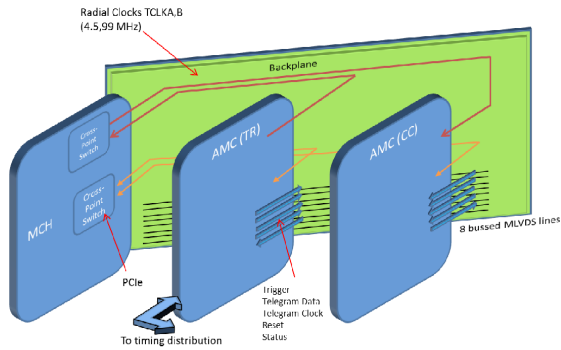
Fig. 3. Connections between the MCH, TR board and the CC board on the MTCA.4 backplane

At the detector end there are FEE units which transport the detector data to the train builder (TB) which in turn sends its data to the PC farm [5]. The CC system multiplies the bunch clock received from the TR to 99 MHz and distributes this clock to the FEE units in order to synchronise the DAQ system to the EuXFEL facility timing.

The clocking circuitry (Fig. 4) on the RTM includes a local crystal oscillator, PLL and non-PLL based multiplexers in order to provide an uninterrupted, stable clock to the final PLL which multiplies the bunch clock to provide the 99 MHz clock. This clock is then converted to differential and goes into a 1:16 LVDS fan-out chip. A copy of this clock also goes back to the FPGA through the RTM connector.
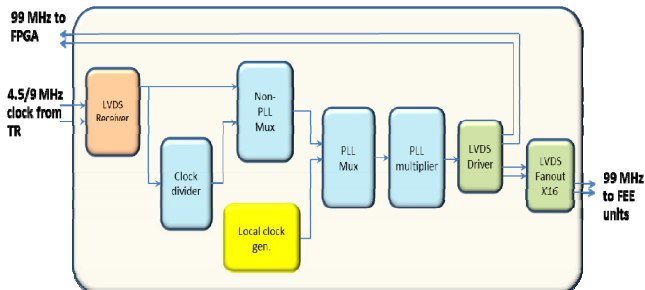

Fig. 4. Block diagram of the clocking circuitry on the CC RTM

The link between a FEE unit and the CC system consists of 4 LVDS pairs which fit into a single RJ45 connector. In addition to the 99 MHz clock, control data and the VETO information are sent to the FEE units. The control data which is called the FAST data contains synchronising information such as the start and the end of a bunch trains along with the train ID numbers and the bunch pattern index values. The status information from the FEE units is received on the remaining differential link.

One CC RTM can support up to 16 FEE units which in turn support a 1 megapixel detector. The system is scalable such that by the use of CC slaves in a single 12 slot MTCA.4 crate, up to 6 megapixel detectors can be supported.

II. THE FPGA FIRMWARE

The FPGA firmware for the CC system is built around a bus/register structure called the II Bus [6], whose registers are accessed through either the PCIe link to the crate processor or the functional blocks attached to the bus as shown in Fig. 5.

The EuXFEL central software system controls the CC system through the PCIe link.
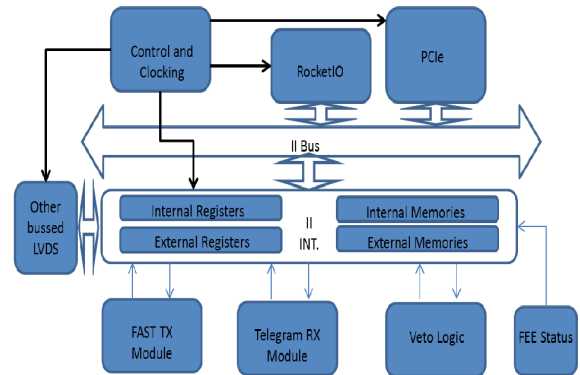

Fig. 5. The block diagram of the CC FPGA firmware

The FAST TX module generates the control messages to the FEE units (FAST data). The protocol for the messages can be seen in table I. These messages are sent synchronously to the 99 MHz clock. The values for the payload are read from the II Bus and the messages are synchronised to the command signals coming from the TR board through the MLVDS links on the MTCA.4 backplane.

TABLE I. THE PROTOCOL FOR THE FAST DATA

Command	Start Bits	Payload	Purpose
START	1100	Train ID (32 bits) + Bunch Pattern Index (8 bits) + Checksum (8 bits)	Notifies FEE of coming train
STOP	1010	None	Notifies FEE that the train ended
RESET	1001	None	Reset FEE
Reserved	1111		

The telegram RX module receives the telegram data from the TR board on the same crate in order to extract the train ID numbers and the bunch pattern index values from the serial data received synchronously to a 130 MHz telegram clock. These values are written to the respective registers on the II Bus.

The veto system for the 2D detectors takes the information from the veto sources and sends commands to the FEEs in order to skip the detector data related to particular bunches. This saves storage in the detector head ASICs for the best results [7]. The veto sources can be avalanche photo diodes, machine protection system and so on. Between the veto sources and the FEEs there are two functional entities, namely the veto units and the veto sources.

The veto logic module in the CC firmware can act as both the veto unit and the user or just the veto user. The function of the veto unit is to gather the data coming on the SFP inputs through the RocketIO module from the possible veto sources and make veto decisions on which bunch data is to be rejected by the FEEs. The veto unit receives the data from the veto sources through 2.5 Gbps high speed serial optical links with a low overhead higher level protocol. The data incorporating the veto decisions are sent to the veto users on the identical physical layer with a different high level protocol.

The veto user processes the information from the veto unit and formats this data to be sent synchronously to the 99 MHz clock to the FEE units. This protocol is shown in Table II.

The veto unit for the 2D detectors is envisaged as a separate MTCA.4 board [7]. However, until the hardware for this unit is developed, the CC system will act as both the veto unit and the veto user. Either acting solely as a veto user or both the veto unit and the user, the CC system will make use of the high speed RocketIO links on the FPGA and the SFP modules that can be attached to the DAMC2. The II Bus registers provide the link between the veto logic and the RocketIO block.

In addition to the modules shown in Fig. 5, further test related modules can be attached to the II Bus such as the PRBS generator block which can be used to test the data link.

TABLE II. THE PROTOCOL FOR THE CC FEE VETO LINK

Command	Start Bits	Payload	Purpose
VETO	110	Bunch ID (12 bits) + 0000	Identifies bunch ID to be vetoed
NO VETO	101	Bunch ID (12 bits) + 0000	No veto defined for that bunch ID
GOLDEN	111	Bunch ID (12 bits) + 0000	Identifies bunch as golden
Reserved	100	Bunch ID (12 bits) + 0000	

III. TESTS WITH THE SYSTEM

The first prototype of the CC system has been manufactured and the initial tests and the system performance tests have been performed.

A. Initial Tests

The first tests with the CC RTM involved ensuring the correct power-on when coupled with the DAMC2 in a MTCA.4 crate. The AMC board turns the 12 V power for the RTM on when the FRU record for the RTM is checked by the MCU and access to the I2C extender is established in order to read the status signals according to the MTCA.4 standard. The MCU then enables the DC-DC converter on the RTM in order to generate the power for the 3.3V voltage rail. The power-on tests for the first manufactured RTM initially failed because of several reasons. At first the 3.3V management power for the MTCA.4 specifications related circuitry was not turned on. This was due to the incorrect values for the timeout capacitors for the hot-swap voltage controller on the DAMC2. Once this was fixed the management power turned on. The faulty soldering of the resistors for setting the I2C address of the I2C extender was the next issue. The MCU's firmware constantly checks the levels on the pins of the I2C extender. When it cannot access this information the 12V to the RTM is turned off. Again this was fixed and 12V to the RTM was turned on once the AMC handle was pushed in. The last problem involved faulty soldering of the DC-DC converter on the RTM on the first prototype board tested. The DC-DC converter on this board was removed allowing other tests which will be presented next. The other prototype boards did not show this problem and generating the main 3.3 V power went smoothly.

After the initial tests the operation of the clock circuitry was tested. As can be seen in figure 3 there are two ways of generating the 99 MHz FEE clock. The first involves the local

oscillator generating 9 MHz and the final PLL multiplying it. The second is to get the 9 MHz or 4.5 MHz clock from the TR board through the TCLK1 line on the MTCA.4 backplane. Verifying the operation of the clock circuitry also tests the RTM connection to the FPGA on DAMC2 as the PLL multiplier is configured by the FPGA and the 99 MHz clock generated also goes back to the FPGA. As a result of the tests the 99 MHz clock was generated successfully from both the clock sources without any problems.

B. Clock Jitter

One of the most important performance metrics for the CC system is the jitter on the 99 MHz FEE clock. This clock is the only clock that provides the synchronisation of the FEE units with the main EuXFEL facility timing. The jitter for this clock was measured using an Agilent MSO scope with the Agilent supplied jitter analysis software EZJIT. The test points on the PCB which are placed on the first output of the 1:16 LVDS fan-out chip just before the RJ45 connector are probed by a differential probe. The types of jitter measured are the Time Interval Error (TIE) and the period jitter.

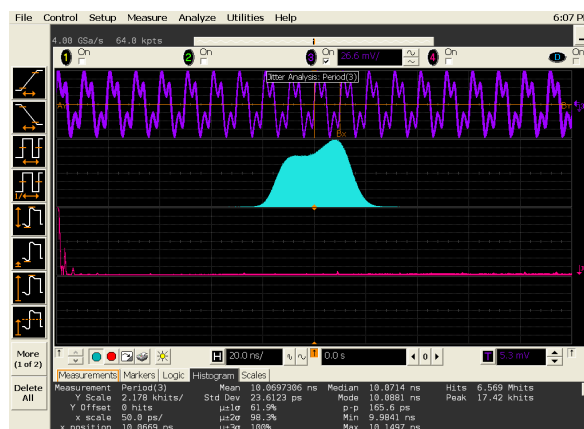Fig. 6: The scope snapshot showing the TIE on the 99MHz clock

Fig. 7. The scope snapshot showing the period jitter

The current configuration of the CC RTM showed a high TIE and period jitter reading on the 99 MHz clock with the shape of the histogram suggesting a high amount of deterministic jitter. The jitter spectrum gives clues about the main source of the jitter. Fig. 6 and Fig. 7 show the TIE and

the period jitter snapshots from the scope. The scope screen is divided into three parts where the top part shows the clock waveform, the middle shows the histogram and the bottom part shows the spectrum of the jitter with the frequency on the horizontal axis and the jitter value on the vertical. Additionally, in the very bottom of the screen statistics for the jitter histogram can be seen. In Fig. 6 there is a high peak around the 780 KHz and a smaller peak at double this frequency. This corresponds to the switching frequency of the DC/DC converter, LTM4600EV, set on the CC RTM. Therefore, we can infer that the main jitter contribution comes from the ripple on the 3.3 V output from the DC/DC converter.

Fig. 8. The TIE snapshot corresponding to the case where 3.3V power is supplied externally.

Another test involved the RTM board with the DC/DC converter removed. We provided the 3.3V from an external power supply with cables soldered on to each side of the output bulk capacitor of the removed DC/DC converter. The resulting TIE and the period jitter measurements showed much improved values, with the jitter histogram suggesting the jitter in the system is mostly random as can be seen from the TIE snapshot in Fig. 8.

The further tests involved applying filtering on the 3.3 V rail to reduce the jitter readings. In order to do this, LTM4600EV was soldered on a small PCB and this PCB attached to the CC RTM by cables so that it received the 12V RTM power from the DAMC2. Fig. 9 shows the most promising jitter readings which were obtained when a LC filter (1uH/1UF) is attached to the output of the DC/DC converter in addition to the required capacitors.
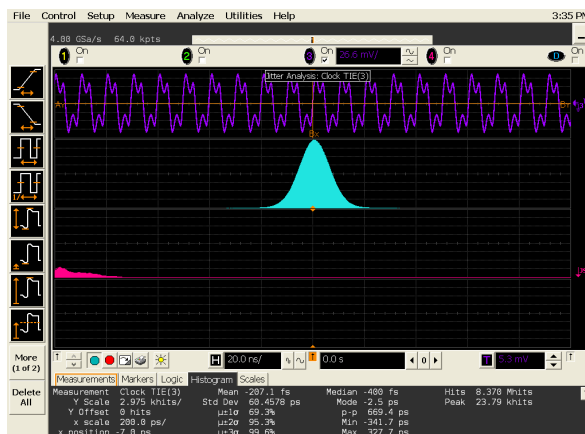

Fig. 9. The TIE snapshot corresponding to the case where the DC converter's output is filtered.

We envisage further improvements when this filtering scheme is employed on the final version of the CC RTM and the voltage plane for the clocking circuitry is separated from the main power plane by a ferrite bead as shown in Fig. 10.
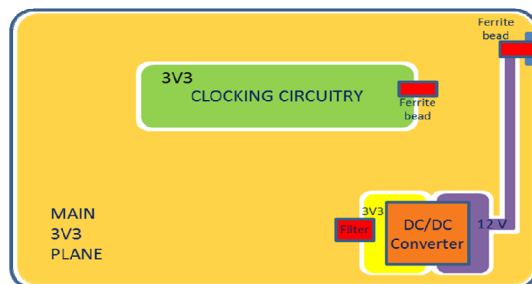

Fig.10. Power supply filtering on the final revision of the CC RTM

C. Cable Length

Reliable data and clock transmission over long cables in the absence of a DC balanced data is an important performance metric. The space limitations in the experimental area necessitate long cable lengths.

The clock and the data links to the FEE units are all AC coupled. Because the data sent to the FEEs is not DC balanced, a special circuitry on the receiver side is used to alleviate the DC wander [8]. As shown in Fig. 11 this circuitry uses a feedback to hold the signal level beyond the RC constant. By having two LVDS buffers in series it limits the data rate and the maximum cable length to be used for the FAST data link.
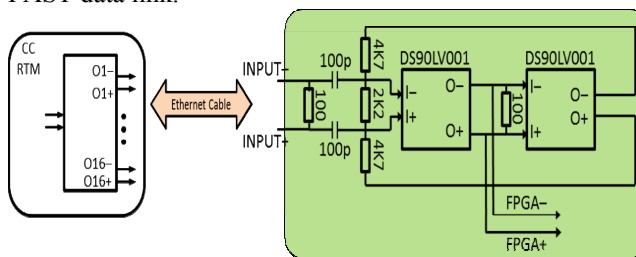

Fig. 11. The receiver circuitry for the AC coupled links on the FEE side

The tests involved using a data pattern which would cause a high DC wander on the AC coupled data link. The data is generated such that short bursts of 22-bit Pseudo Random Bit

Sequence (PRBS) words are interspersed between long sequences ones or zeros. The sequence always starts with a predefined start word for synchronisation. The data is sent in a source-synchronous way to the 99 MHz FEE clock. Fig. 12 presents a scope output showing the clock and the bursts of data.
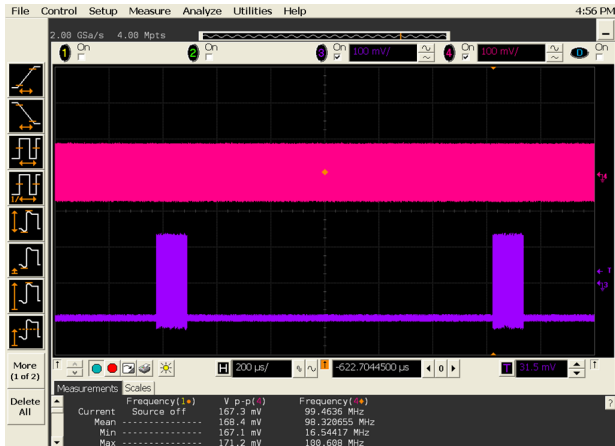

Fig. 12. Scope snapshot showing the PRBS words interspersed with long periods of zero.

The receiving circuitry was realised on a test PCB [9] that would be installed as an extension board to a development board (XUPV5) that houses a Xilinx XV5110T device. Both the clock and the data channels had this special receiving circuitry on the test PCB which also has a RJ45 connector and 100 ohm balanced, length-matched LVDS lines going straight into the FPGA through the daughterboard connector. The receiving circuitry transfers the data to the FPGA on the receiver card and the data is compared to the data generated on the receiver card in tandem. In the receiver firmware there is a word and a bit error counter to observe the error rate. The Chipscope analysis software running on the receiver provides the ability to view the data transmission and the error rate.
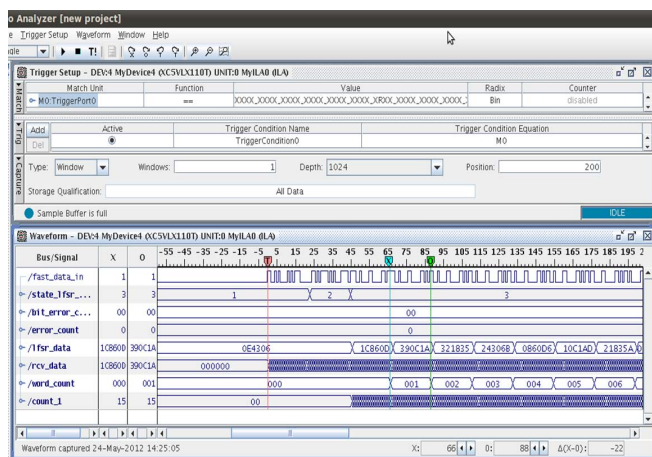

Fig. 13. A Chipscope snapshot from the long cable tests

The tests were performed using Ethernet cables of lengths 10 m, 15 m, 20 m, 30 m and 50 m. There were no errors observed during a running period of more than 24 hours with the CAT6 SFTP cables up to 30m. Fig. 13 presents a Chipscope snapshot from the test with a 30m CAT6 SFTP

cable showing correctly received random data after a long period of zero data. The scope output showing the beginning of the random data signal with the 99 MHz clock is shown in Fig. 14. The random data test failed at the 50 m cable test. The data word denoting the start of the random sequence was not properly captured every time due to the reduced voltage swing at the end of the cable. If there is a need to support a 50m cable length, MLVDS drivers have to be tested for data and clock transmission.
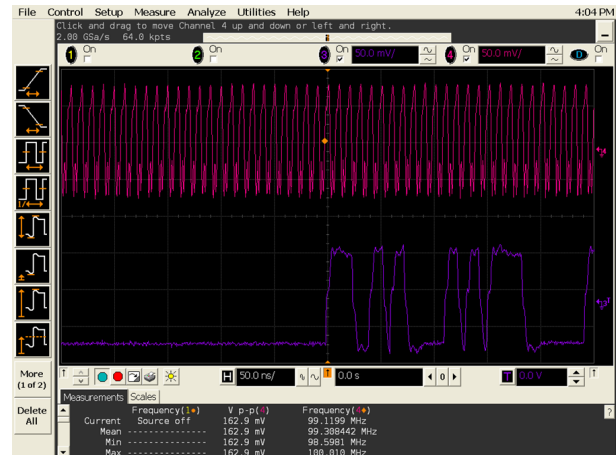

Fig. 14. Scope snapshot showing the start of the random data pattern

IV. Conclusions

The experience with the first prototype of the CC system has been positive, with the solution of using the DAMC2 AMC board as a base unit coupled with the CC RTM proven to be valid.

The performance tests showed that there is a need for improvement especially the jitter readings on the 99 MHz line. Further tests to reduce the jitter value on this clock tell us that this is achievable with the solution of applying a filter at the output of the DC/DC converter and the power plane for the clocking circuitry being separated from the main power plane by a ferrite bead. The required length of the cable between the CC system and the FEEs is not finalised yet, however the system can support up to a 30m cable with the current configuration, albeit in the lab conditions. Further work on improving this performance metric is being undertaken. Additionally, the tests involving the actual FEE hardware and a prototype DAQ system integration test are to be done soon.

The CC hardware/firmware system is designed to provide the flexibility, extensibility and scalability to support possible future upgrades to the 2D megapixel detectors. In light of the observations shown here, we are going to start designing the final version of the CC hardware.

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