Development of the LPD, a High Dynamic Range Pixel Detector for the European XFEL

Mathew Hart, C. Angelsen, S. Burge, J. Coughlan, R. Halsall, A. Koch, M. Kuster, T. Nicholls, M. Prydderch, P. Seller, S. Thomas, A. Blue, A. Joy, V. O'shea, M. Wing

***Abstract*– We present the development and prototype test of the LPD instrument, a novel pixel detector for the European XFEL. At XFEL the LPD detector must be capable of operating with a frame rate of 4.5MHz and record images with a dynamic range of 1:100,000 photons (12keV) whilst maintaining low noise. The prototype LPD system has a large in pixel memory depth of 512 images that can be selected with a flexible veto system. Data is then transferred off the detector head in between XFEL pulses with an accompanying high rate data acquisition system. The system has been prototyped and assembled into an LPD detector head that contains custom silicon sensors and ASICs as well as a programmable data acquisition cards and supporting electronics and mechanics. A second version of the ASIC has also been submitted for manufacture. The experiences with our first prototype are presented.**

I. Introduction

THE Large Pixel Detector (LPD) is being designed and built by STFCs Detector Division for The European XFEL. The XFEL machine will produce tens of thousands of X-ray pulses every second. These bursts of pulses arrive in a regular bunch structure giving a rate equivalent to 4.5 million frames a second during the active burst period. At this speed it will be possible to image chemical interactions as they happen, or measure chemical structures without the need to crystallise the sample. The challenge for the detector system is to record at this frame rate, read all the data out and be ready for the next bunch a tenth of a second later. This is all to be achieved while meeting demanding noise and dynamic range requirements. New detector concepts are required to fulfill this challenge [1]. An LPD system is built around a 4096 pixel detector tile with 500um pixels, many of these units are butted together to form larger area sensors. Bonded to each detector tile are 8 readout ASICs. Each ASIC handles a 512 channel portion of the detector, using 3 parallel gain stages (1x,10x,100x) to achieve the dynamic range and noise requirements. The output from the 3 gain stages is stored to analogue memory with capacity for 512 frames. Following a series of pulses from the XFEL, the stored frames are readout from the on chip memory by 16 SAR ADCs. Data is streamed at high speed using LVDS to a Front End Module DAQ board (FEM) that collects and sparsifies the data. The FEM also serves to control the ASICs. A single FEM board brings together the data from 128 ASICs. This forms the super-module unit from which the system mechanics and support are built around. The super-module is designed such that many super-modules can be combined to form large seamless detector configurations. The current target configuration is a megapixel arrangement with 4x4 super-modules.

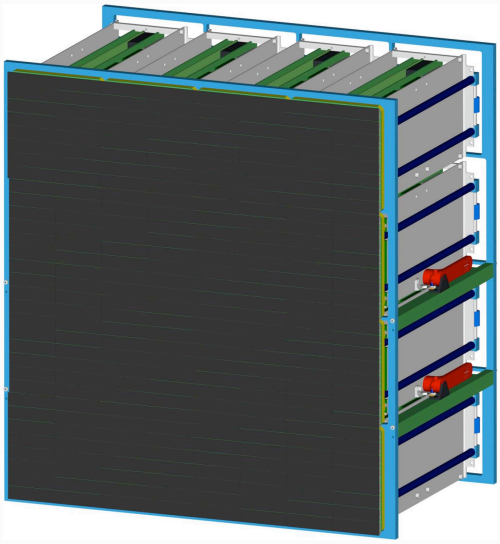

Fig. 1. An LPD 1 megapixel detector will be made from 4 x 4 super-modules.

II. Detector Components

A. Sensors

The sensor material used for LPD is high resistivity silicon. These have been custom made for the LPD system. The detection surface for a large area detector is made up of many tiled units. Each tile has 128 x 32 pixels on a 500um pitch. The thickness of the sensor is also 500um. The backside of the sensor is n+ implanted and aluminized to allow a bias to be applied across the device. On the front side of the device the pixels are tracked to a tighter pitch array for bonding to the readout electronics. The tracking is on a second layer of metal, this can be seen in figure 2.

Manuscript received November 16, 2012.

Mathew Hart, C. Angelsen, S. Burge, J. Coughlan, R. Halsall, T. Nicholls, M. Prydderch, P. Seller, S. Thomas are with the Science and Technology Facilities Councils Rutherford Appleton Laboratory, UK (e-mail: matthew.hart@stfc.ac.uk).

A. Koch, M Kuster, are with The European XFEL. Hamburg, Germany.

A. Blue, V O'shea are with The University of Glasgow, UK.

A. Joy, M. Wing are with University College London, UK.

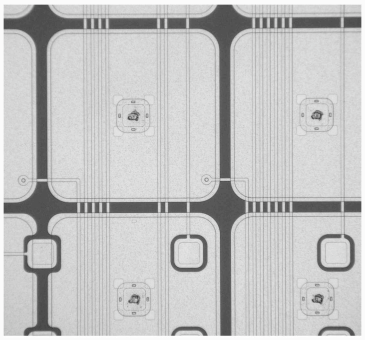

Fig. 2. A close-up image showing part of a sensor. The 500um pixels and tracking to smaller pitched bonding array can be seen.

By reducing the bonding pitch it is possible to hide all the electronics behind the sensors and allow closer positioning of adjacent tiles.

B. *Front end readout ASIC*

When x-rays arrive in the sensor they create electron hole pairs. For a monochromatic source this charge is proportional to the number of x-rays incident on the detector. In LPD this charge is readout by a custom Application Specific Integrated Circuit (ASIC). There are 8 ASICs bonded to each sensor with 512 pixelated readout channels on each ASIC. The ASIC takes advantage of the bunch structure of the European XFEL machine. The images are saved onto the ASIC in analog form at the high frame rate (4.5MHz) during the burst of pulses. Following the burst the analog data is converted to digital and streamed off the ASIC. During image capture the charge readout from the sensor is input into a preamplifier with 50pF capacitive feedback. This is a relatively large feedback capacitance and gives a high dynamic range of 10^5 12keV photons. This amplifier has a dynamic slew correction circuit to allow the reset of such a large capacitance [2]. Following the preamplifier there are a series of parallel gain stages. For the smallest signals an amplifier with 100 gain is used to boost the signal. An intermediate gain of 10 is used for mid-range signals and a unit gain amplifier is used for the largest signal levels. The appropriate gain level for each pixel is selected at a later stage. If the user knows they will not need the full dynamic range there is also an option to switch the preamplifier feedback to a 5pF option giving a boost to the signal to noise of the system at the expense of dynamic range.

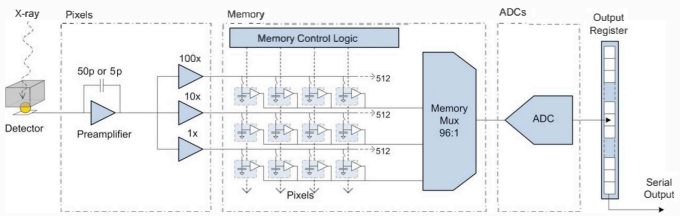

Fig. 3. A simplified schematic of the ASIC architecture.

The outputs from the gain stages are saved to 512 channels of analog memory. The memory is controlled by a command interface that allows the user to veto frames they deem not to be of interest and allow them to be overwritten. This makes better use of the memory available. The same command interface is also used to drive the ASIC through various states from image capture to data readout. This allows the system to be very adaptable should requirements change. During the readout phase 16 on chip ADCs convert the data in the analog memory and stream it off the ASIC at 100MHz via a LVDS output.

The first version of the ASIC did not meet the noise requirements for single photon resolution. There were also some issues identified with radiation hardness of some circuit blocks. The ASIC has been modified to make improvements to the noise performance and increase radiation hardness. The new design has been submitted and is in manufacture.

C. *Interconnect*

The Sensor tiles and ASICs are bonded together using gold stud to Silver loaded epoxy. Between the two layers we have a silicon interposer with through vias for every pixel. This serves to put some vertical space between the ASIC and sensors which allows the regular wire bonds for the ASIC to be hidden behind the sensor. This stack of interconnect can be seen in figure 4. The image shows a complete detector tile with one 4096 channel sensor and 8 readout ASICs.

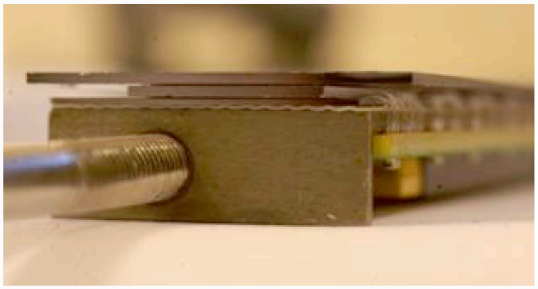

Fig. 4. A side view of a bonded detector tile. From top to bottom: Sensor, Interposer, ASIC, Molybdenum support block.

This 4 side buttable detector tile is then used to build up large areas with multiple units. 16 detector tiles are used to make a Super-module, which is the building block for larger systems. A Super-module can be seen in figure 5. The gap between active areas is 4 pixels on each side of tile. This is equivalent to 13.8% dead area.

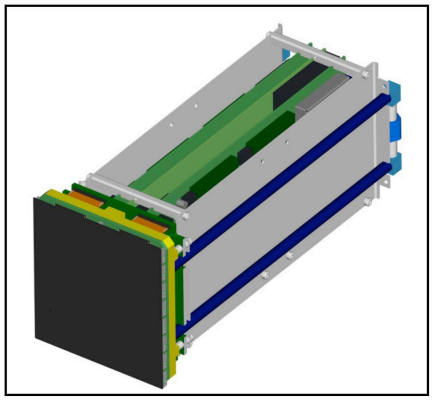

Fig. 5. A mechanical drawing of the Super-module. Larger detector system are built using multiple units.

D. Data Acquisition

The data from the ASICs is captured by the Front End Module (FEM) data acquisition card. The FEM also sends commands and setting to the ASICs to control their operation. A FEM connects to 16 detector tiles corresponding to ~65,000 pixels. Figure 6 shows an image of the complete FEM board.

Fig. 6. The FEM DAQ board.

It is built around a Xilinx Virtex 5 FPGA, this is the main processing unit on the board. With all channels running full speed the data rate into the FEM is 12Gbps. The FPGA is programmed to perform tasks such as the data sparsification in choosing the correct gain level for each pixel. Data is output to the next layer of the system via 10Gbps Optical Links on a mezzanine card attached to the FEM. This can either be to a standalone PC or to the Train Builder [3] that collates the data from multiple FEMs. The control path to the FEM is via a Gb Ethernet connection and a clock and control port that synchronizes the system to the XFEL machine.

E. Power Card

A Super-module contains 2 power cards. Each one serves 8 detector tiles providing around 2.5 volts at 64 A for the readout ASICs. A dedicated regulator unit supplies each detector module. These can be seen on the board in figure 7. The power card also provides the detector bias voltage applied across the sensor silicon and powers the FEM board. The power card features temperature monitoring circuits for the detector tiles it powers and local board monitors.

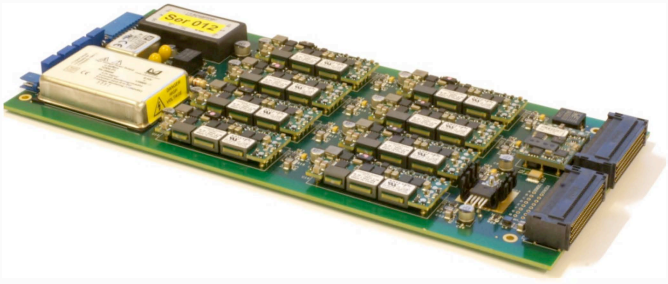

Fig. 7. The LPD power card.

F. Mechanics

The Super-modules are assembled into larger systems using mechanical frames. These are designed to allow the Super-module to be loaded easily into the detector from the front face. The spacing between each super module is such that the number of missing pixels between detector tiles on adjacent Super-modules is the equal to that between tiles on the Super-module.

A quarter megapixel frame has been manufactured that contains 4 Super-modules. This prototype housing can be seen in figure 8.

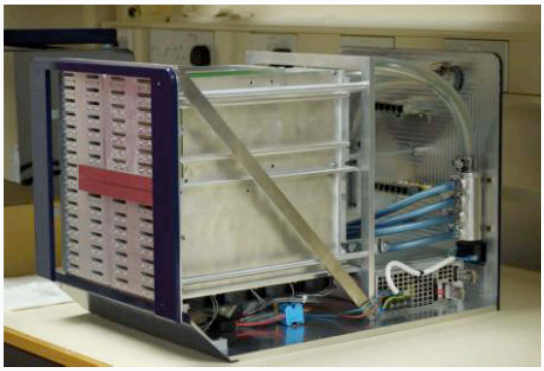

Fig. 8. A quarter megapixel housing with 4 Super-modules inserted. 6 detector tiles have been added, partially populating the detector.

III. Test Results

A single detector tile has been tested on an x-ray set with a flood illumination and rotating chopper wheel. This both demonstrated the high frame rate of the system and quality of the interconnect used to construct the module. The x-ray set has limited brightness so the system was run slower to get a good signal. Tests were run at 4.5kHz and 3.6MHz. Figure 9 shows a frame taken in the 4.5kHz tests.

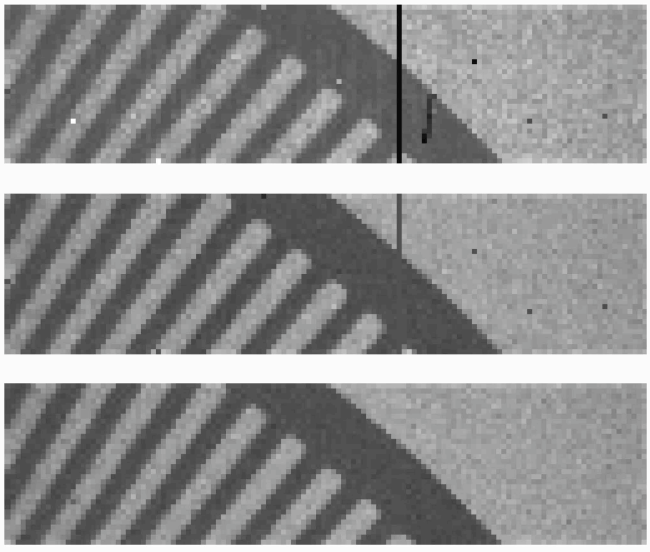

Fig. 9. An image taken with the system on an x-ray set. From top to bottom: Raw data, corrected for pedestals, corrected for bad pixels.

The first image is raw data with no corrections. In the second image pedestals have been subtracted from the data. This clears some artifacts. In the final image bad pixels and columns have been removed. These bad pixels are due to

unconnected bonds between the ASIC and sensor. The bad column is due to a defective ADC on that ASIC. The cluster of dark pixels is due to a short in the interposer that sits between the sensor and ASIC. This disappears when pedestals are subtracted.

IV. Conclusions and Next Steps

We have designed, built and demonstrated all the components to build large area pixelated detectors that match the demanding requirements of the European XFEL.

In the near future the revised ASIC will arrive with improved noise performance and increased radiation hardness. This ASIC will be built into new detector tiles that can be used to populate the Super-modules in the larger systems such as the quarter megapixel LPD system. Test of the system is planned to take place on a beam line at PETRA III. There the full dynamic range of the system can be tested.

In the longer term a 1-megapixel housing is to be developed and the manufacture of the components to populate it will commence. The work is scheduled to deliver this system to the European XFEL ready for the first user experiments.

Acknowledgment

The authors would like to acknowledge the work done at UCL by Matthew Wing and Ashley Joy on simulations of the detector image output. Also to the European XFEL for funding the work and their continuous support and advice.

References

[1] H. Graafsma, “Requirements for and development of 2 dimensional X-ray detectors for the European X-ray Free Electron Laser in Hamburg," *2009 JINST 4 P12011*.

[2] H.M.D. Ip, S. Thomas, M. Hart, M. Prydderch, M. French, "A Dynamic Slew Correction Circuit for Low Noise Silicon Detector Pre-amplifiers," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 3, pp. 642-646, Jun. 2012.

[3] J. Coughlan, C. Day, S. Galagedera, R. Halsall, “The Train Builder data acquisition system for the European-XFEL," *2011 JINST 6 C11029*.