Slab Data Paths
A Resumé

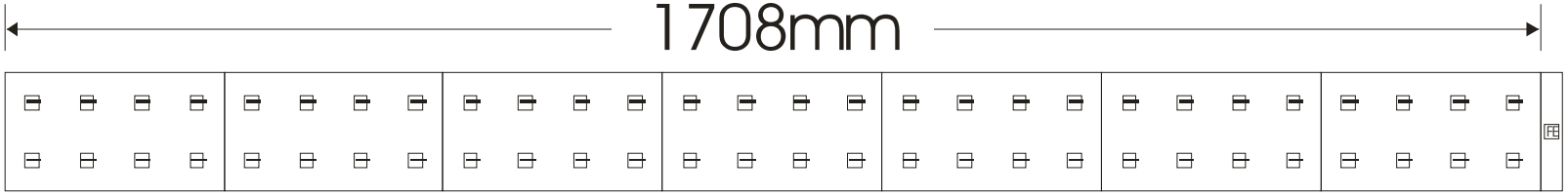
Maurice Goodrick
University of Cambridge

Overview

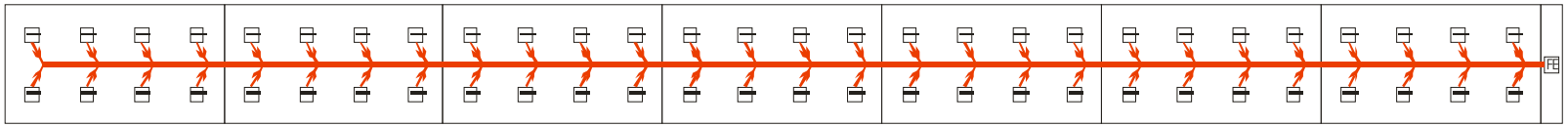
- The Task
- Moving Parameters
  - And how to fix them
- Copper Links and Power Budgets
  - LVDS, etc
  - Structured Readout
- CMOS Traces
  - CMOS Power Budget
  - How much capacitance
    - *PCB Build*
- Plans
  - Test Slab: PCB-0

A Typical SLAB

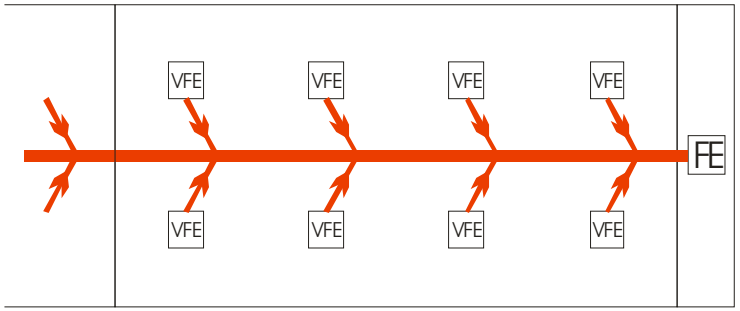
CALICE_MJG



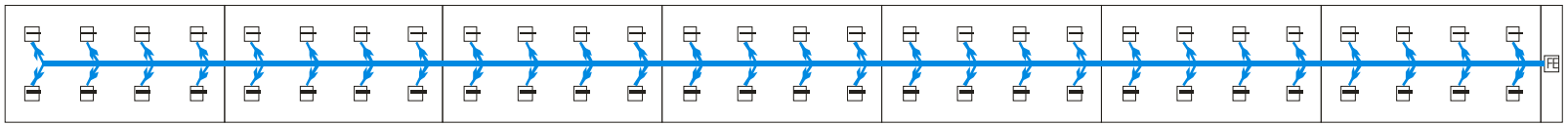
Just One Side of the SLAB!!



Read Out



Clock & Control

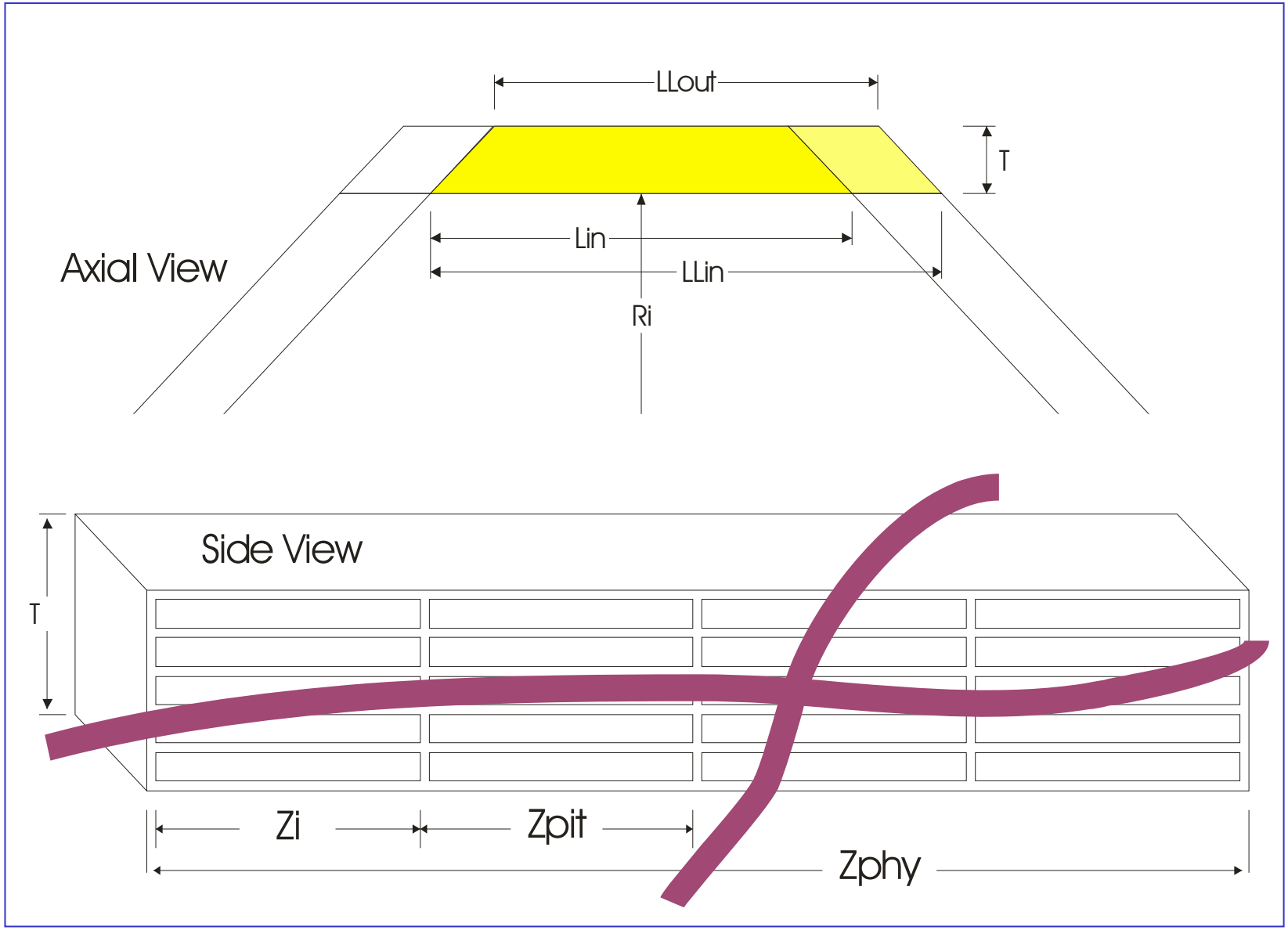


Beam Parameters

Parameter	Beam Scenarios		
	B1	B2	B3
BX Period (ns)	176	176	
# BX per Bunch	4886	9772	
Bunch Duration (us)	860	1720	0
Bunch Period (ms)	250	250	

CALICE Geometry

CALICE_MJG



Calice Parameters

Parameter	CALICE Scenarios		
	CG1	CG2	CG3
Radius (inscribed) Ri (mm)	1700	1600	1600
Thickness T (mm)	200	200	200
Znom - Nominal Length along Beam axis (mm)	5500	4360	4360
# Slabs per Stack	15	15	15
Zi - Slab Width (Instrumented) (mm)	120	120	120
Zpit - Slab Pitch along Beam axis (mm)	122	122	122
# Slabs along Z (Nominal)	45.1	35.7	35.7
# Slabs along Z (Nearest Int)	45	36	36
Zphy - Physical Length along Beam axis (mm)	5490	4392	4392
# Slabs Total	5400	4320	4320
Lin - Inner Polygon Side (mm)	1408	1325	1325
LLin - Inner Instrumented Slab Length (mm)	1691	1608	1608
LLout - Outer Instrumented Slab Length (mm)	1291	1208	1208
LLav - Average Instrumented Slab Length (mm)	1491	1408	1408
# Pads per cm^2	1	1	4
# Pads per Slab (nominal)	4000	3840	15360
# Pads per Average Slab (estimated)	3576	3384	13536
# Pads Total (Millions)	19.3	14.6	58.5

Data Rates

Parameter	
# Bytes per Pad (non-Z Suppressed)	2
# Bytes per Pad (Zero Suppressed)	4
Zero Suppression factor	100

Parameter		Scenarios		
	ReadOut:	R1	R2	R3
	Beam:	B1	B1	B1
	CALICE:	CG1	CG2	CG3
# BX per Bunch		4886	4886	4886
# BX per Sec		19544	19544	19544
# Pads per Average Slab		4000	3840	15360
# Bytes per BX	Per Slab non-Z Suppressed	8000	7680	30720
# MBytes per Bunch Train		39.1	37.5	150.1
# MBytes per sec		156.4	150.1	600.4
# Mbits per sec		1564	1501	6004
# Bytes per BX	Per Slab Zero Suppressed	160.0	153.6	614.4
# MBytes per Bunch Train		0.78	0.75	3.00
# MBytes per sec		3.13	3.00	12.01
# Mbits per sec		31.3	30.02	120.08

Copper Links - LVDS

CALICE_MJG

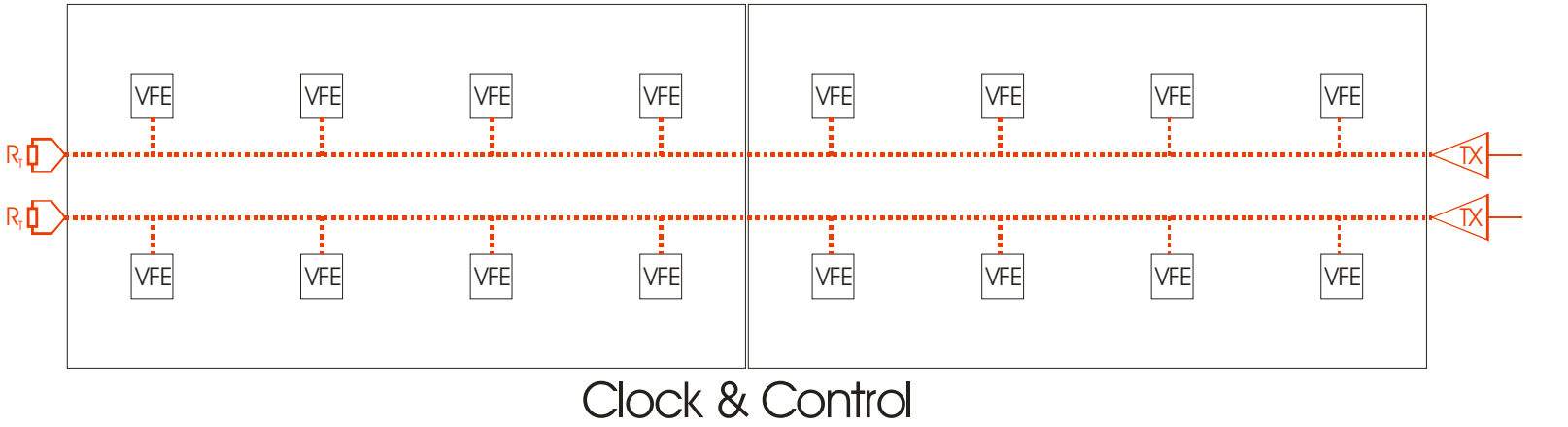
		LVDS Figures						
Vcc	3.3							
Driver Device	DS90LV031A				Link Speed (Mbit/s):			
					20	40	100	200	400
Current for Quad (mA)					21	21	22	23	25
Power for Quad (mW)					69	69	73	76	83
Current per Link (mA)					5.3	5.3	5.5	5.8	6.3
Power per Link (mW)					17.3	17.3	18.2	19.0	20.6

	Scenarios			Rate Needed	Rate (Mbit/s):				
	ReadOut	Beam	CALICE	(Mbit/s)	20	40	100	200	400
#Links needed per Slab / Usage of Link	R1	B1	CG1	31.3	1.56	0.78	0.31	0.16	0.08
	R2	B1	CG2	30.0	1.50	0.75	0.30	0.15	0.08
	R3	B1	CG3	300.2	15.01	7.50	3.00	1.50	0.75
Links Power per Slab (Av) (mW)	R1	B1	CG1	31.3	27.09	13.54	5.68	2.97	1.61
	R2	B1	CG2	30.0	26.00	13.00	5.45	2.85	1.55
	R3	B1	CG3	300.2	260.04	130.02	54.49	28.48	15.48

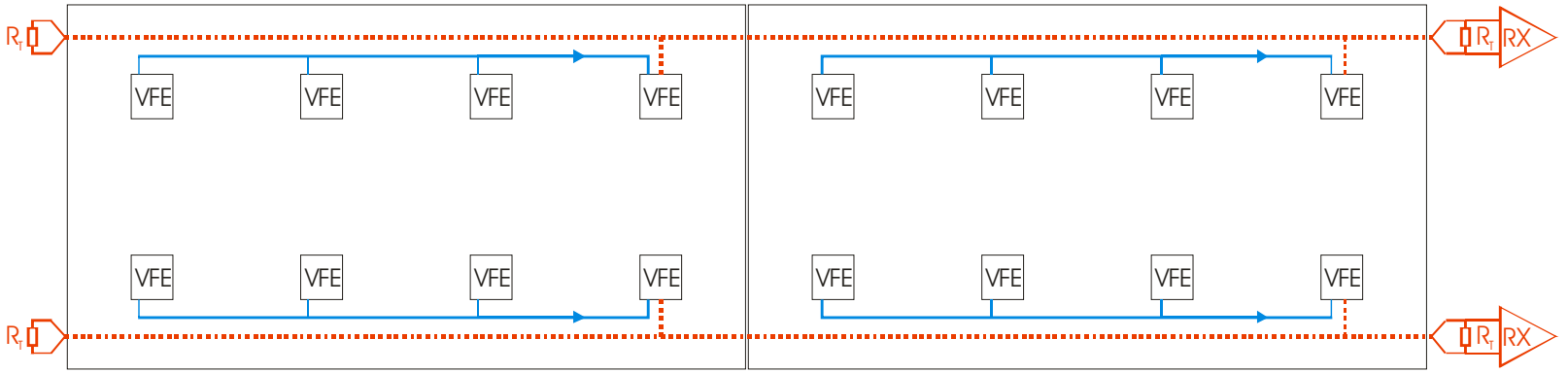
Fast Links with low duty cycle are power efficient
May allow more links, giving structured R/O
But … are such speeds achievable?
CML may be good alternative
Self-clocking – SERDES, etc
Clock and Control Link

Signal Routing

2-Tier Structure for Read Out



Clock & Control



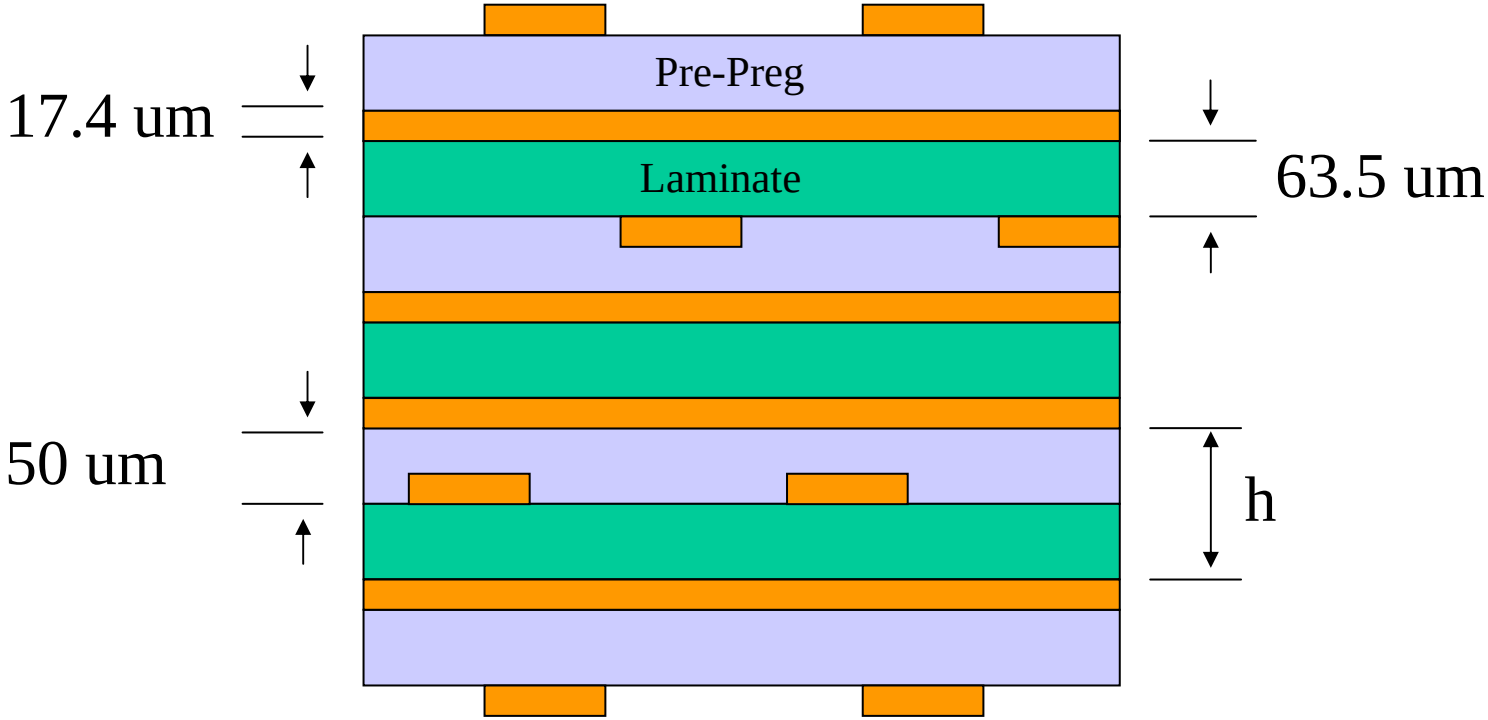
Read Out

CMOS Links
Power Budget

			CMOS Figures		
Vdd	3.3				
Signal Swing (V)	2.5				
Load Capacitance (pF)	5				
Area per ASIC (cm^2)	36				
# ASICs in Read Out Group	4				
			ReadOut Scenario		
Charge per Transition (pQ)		12.5			
Dissipation per Transition (pW)		41.3	R1	R2	R3
Pads per ASIC			36	36	144
# Kbits per sec per ASIC Group (Zero Sppressed)			901	901	3602
# +ve edges/s/ASIC Group (Zsup) (K)			225	225	901
Dissipation per ASIC (uW)			2.3	2.3	9.3

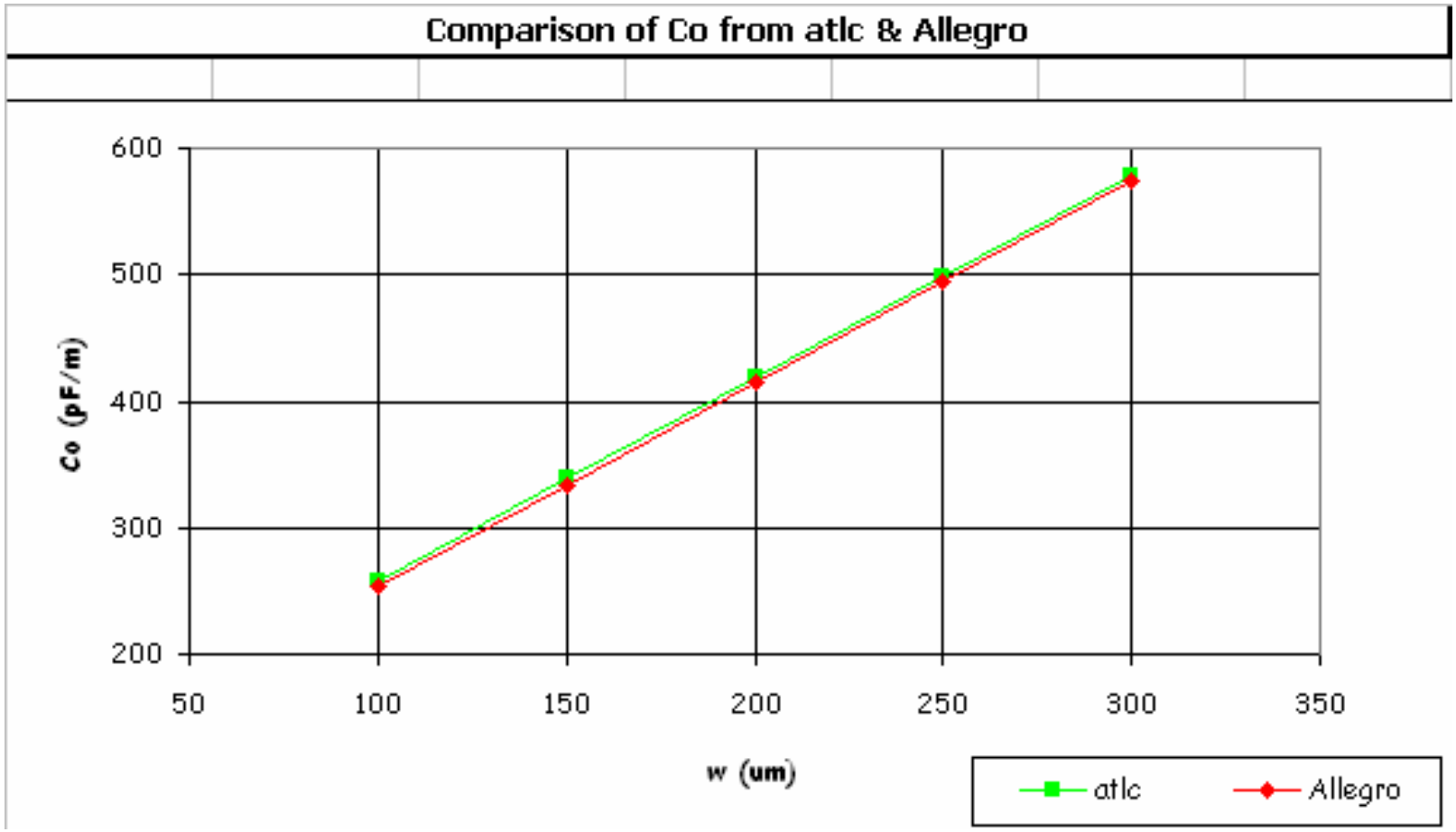
But what is the capacitance ??

8 Layers in 600um !! - NOT TRIVIAL



Approximate to Cu central in h = 113 um dielectric

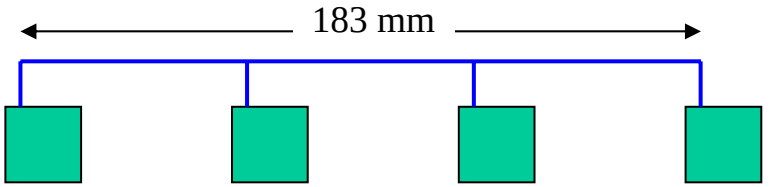
Cadence Allegro & atlc



With the invisaged build and with w ~ 200 um, Co =~420 pF/m

If Track Length ~ 200 mm,

C ~84 pF



			CMOS Figures		
Vdd	3.3				
Signal Swing (V)	2.5				
Load Capacitance (pF)	84				
Area per ASIC (cm^2)	36				
# ASICs in Read Out Group	4				
			ReadOut Scenario		
Charge per Transition (pQ)		210.0			
Dissipation per Transition (pW)		693.0	R1	R2	R3
Pads per ASIC			36	36	144
# Kbits per sec per ASIC Group (Zero Sppressed)			901	901	3602
# +ve edges/s/ASIC Group (Zsup) (K)			225	225	901
Dissipation per ASIC (uW)			39.0	39.0	156.0

This is < 2 uw/pad – 2% of budget

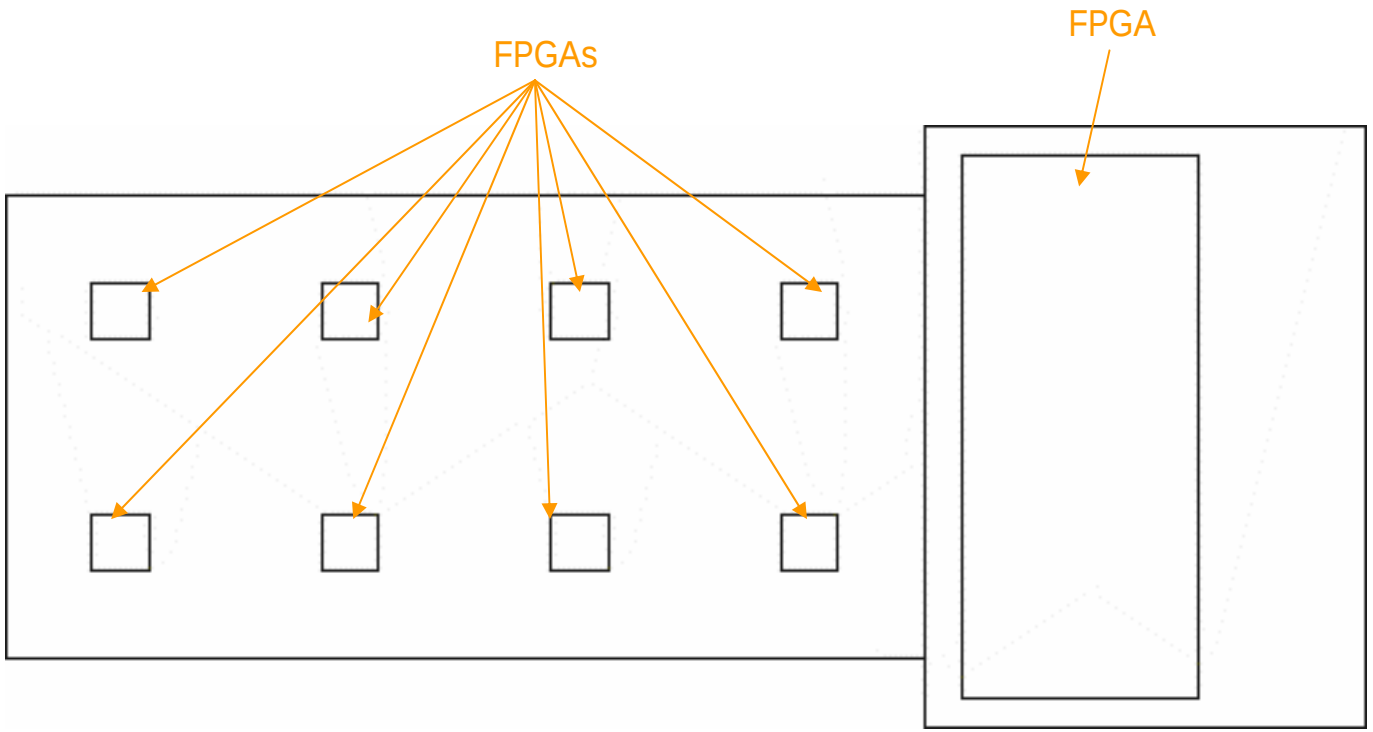
Driver Specification

Reduced speed => less crosstalk and noise

- @ 1 Mbit/s, T = 1 us ... allow $t_r = t_f$ = 100 ns ??
  - Driver current: $i = C.\Delta V / t_r$
    - *if C = 84 pF, ΔV = 2.5 V, gives* **i = 2.1 mA**
  - Driver R_S: $R_S = t_r / 2.2\,C =$ **~ 540 Ω**
- @ 3.6 Mbits/s, need $t_r = t_f$ = 30 ns, giving:

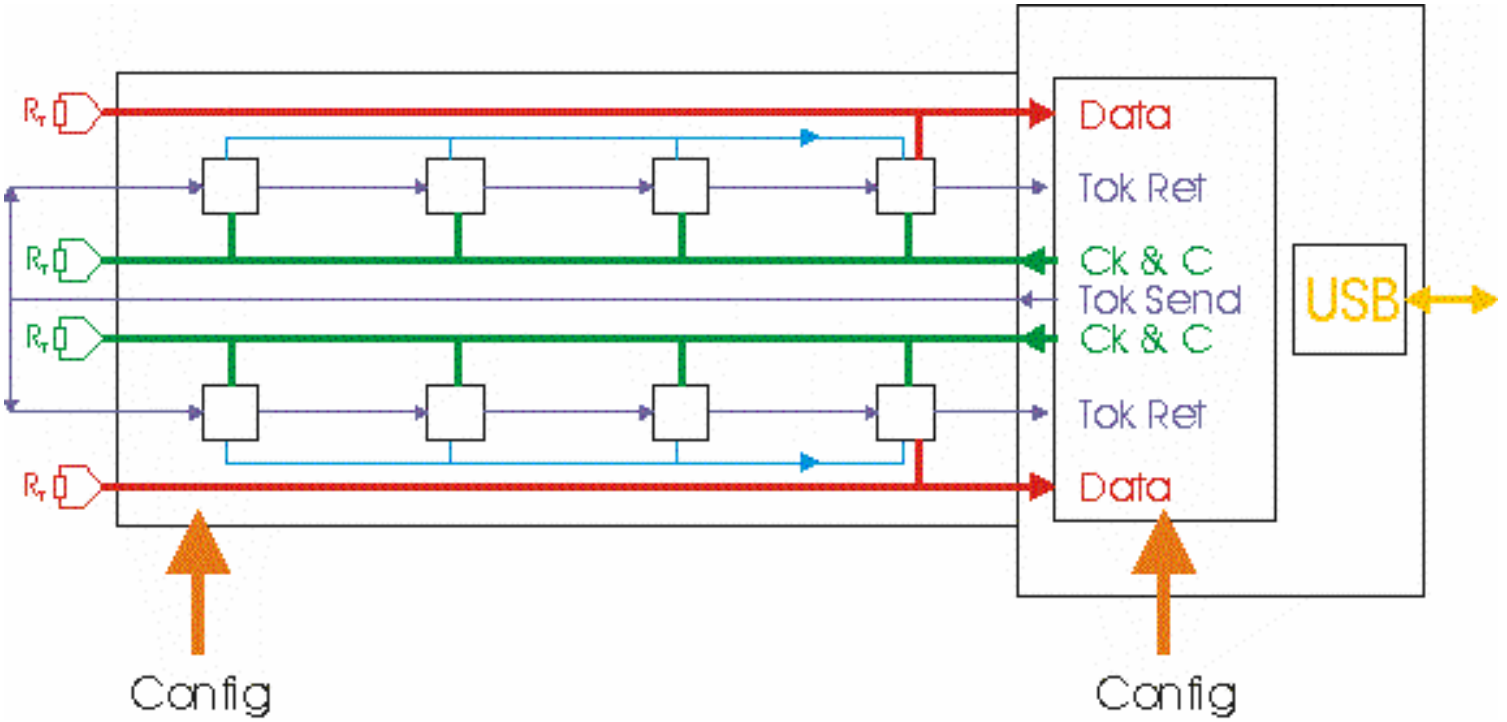
i = 7 mA and **R_S ~ 160 Ω**

PCB-0 Layout



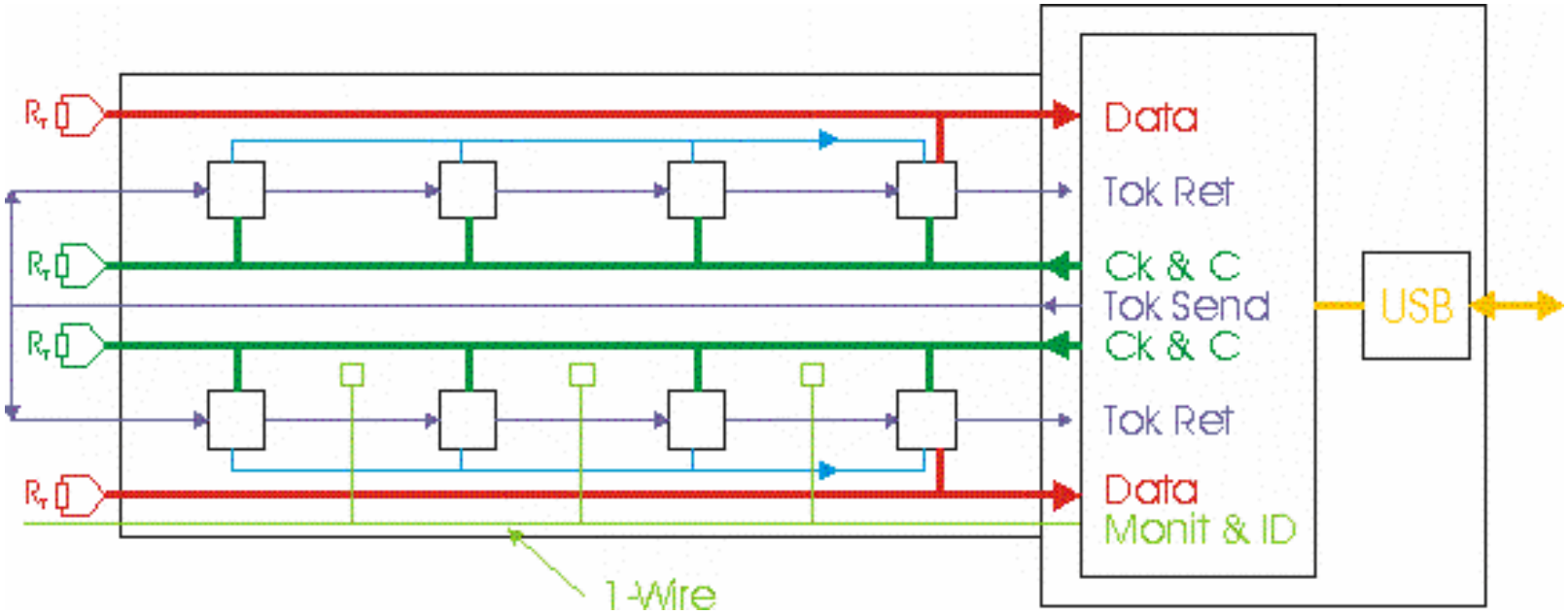
PCB-0 Data Paths

- Composite Clock and Control
- 2-Tier Data Paths?
- Token for Raed Out?
- Configuration … model UCL plans for secure configuration?
- USB

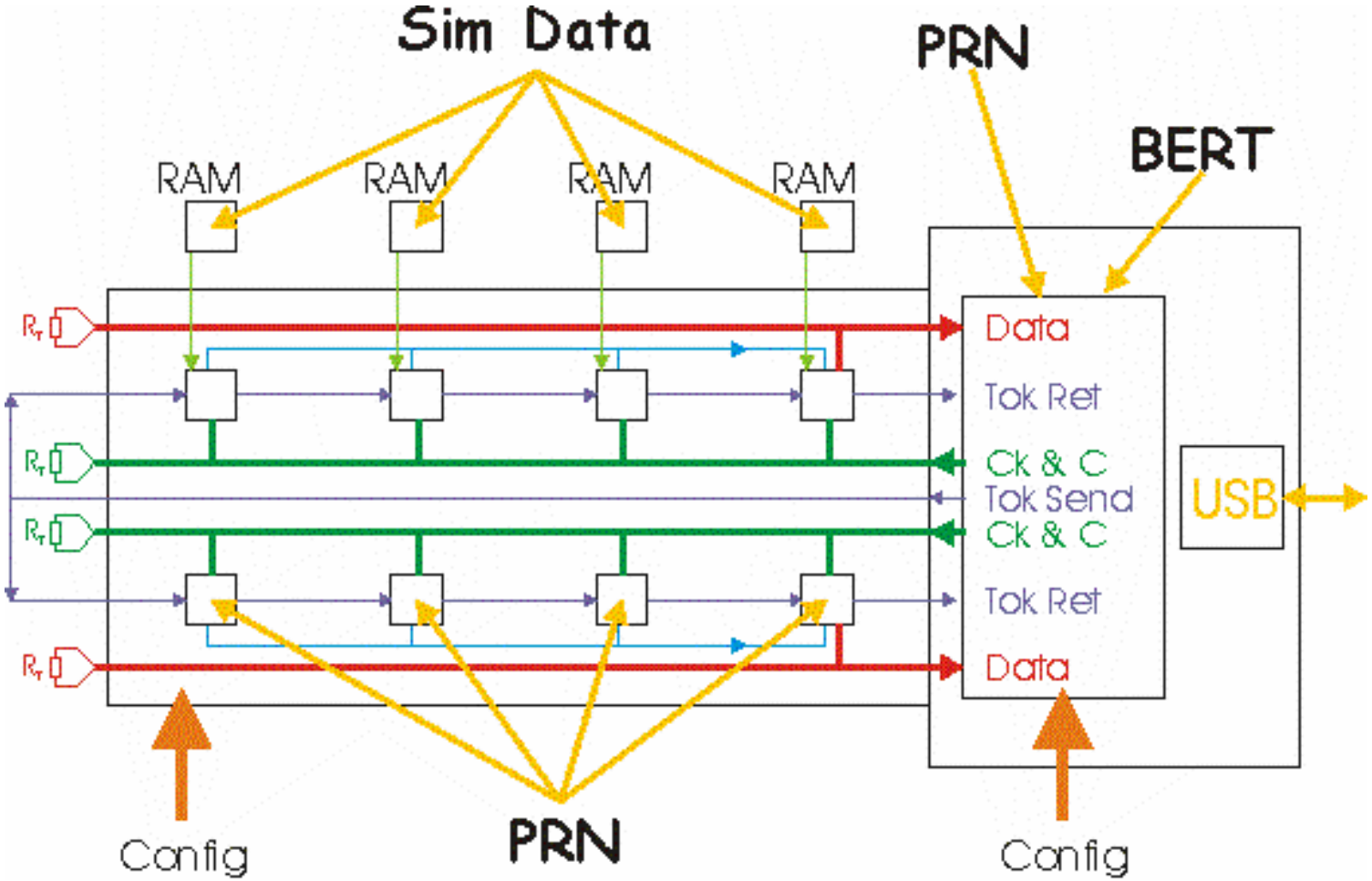


Monitoring

- Temp
- Supplies
- Ident



PCB-0 - Functions



Summary

- Copper Read Out not easy even with Zero Suppression
  - 50 times worse without!!
  - But are there cheap, available, proven alternatives ??
- Clock with Data for Read Out and Clock & Control ??
  - Encoding and sending sounds OK
  - But RX function in VFE ASIC ?? (limiting amps, PLLs, keeping jitter low ??)
- Redundancy:
  - Architecture
  - Effect on power budget
  - Do we mind if ASIC in Read Out group is lost (144 cm^2)
  - Do we really mind if a slab is lost?
- Joints between panels:
  - hard to model until ideas have firmed up
- Lots to do, limited time
  - Need to be able to provide input to VFE design which freezes mid 2007